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Pulse width and height modulation for multi-level resistance in bi-layer TaO_x based RRAM

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Multilevel switching in resistive memory devices enables a wide range of computational paradigms, including neuromorphic and cognitive computing. To this end, we have developed a bi-layer tantalum oxide based resistive random access memory device using Hf as the oxygen exchange layer. Multiple, discrete resistance levels were achieved by modulating the RESET pulse width and height, ranging from 2 kΩ to several MΩ. For a fixed pulse height, OFF state resistance was found to increase gradually with the increase in the pulse width, whereas for a fixed pulse width, the increase in the pulse height resulted in drastic changes in resistance. Resistive switching in these devices transitioned from Schottky emission in the OFF state to tunneling based conduction in the ON state, based on I-V curve fitting and temperature dependent current measurements. These devices also demonstrated endurance of more than 10⁸ cycles with a satisfactory R_{off}/R_{on} ratio and retention greater than 10⁴ s. *Published by AIP Publishing.*

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Resistive Random Access Memory (RRAM) devices, which are commonly referred to as memristors, are strong candidates for replacing existing non-volatile memory (NVM) options, such as flash. According to ITRS 2015, Resistive RAM (RRAM) devices have been categorized as one of the leading emerging memory devices for NVM. RRAM has drawn considerable attention among researchers as a potential candidate for next-generation non-volatile memory, due to its simple structure, fast switching speed,¹ endurance, and retention.² The basic structure of RRAM is a Metal-Insulator-Metal (MIM) structure where single or multi-layers of insulators are sandwiched between two metal electrodes.

Besides down-scaling of memory cells, another effective way to increase the memory density is to store more information in a single device. This is commonly referred to as multilevel cell (MLC) storage. For RRAM, multilevel resistive switching has been demonstrated in previous reports by setting the current compliance,³ changing the RESET voltage,⁴ and modifying the amplitude of the voltage pulse;⁵ however, many of these reports have not shown sufficient endurance of switching within these states or suffered overlap between the states, which can lead to bit read errors.

In this study, we demonstrated multilevel resistance states in a W/Hf/TaO_y/TaO_x/Pt RRAM device by changing the RESET pulse width and height. Hf is placed between the top electrode and the oxide as an oxygen exchange layer (OEL) to scavenge oxygen and thereby modify the stoichiometry of the oxide. As Hf has lower electronegativity (1.23), it can interact more strongly and effectively with oxygen ions nearby the interface, producing a high oxygen vacancy concentration at the Hf/TaO_x interface and making that interface quasi-ohmic. Oxygen transfer from the oxide to Hf layer can be explained in terms of thermodynamic driving force (Gibbs free energy). Gibbs free energy for oxide formation of Hf (−1010 kJ/mol) is lower than that for Ta (−760 kJ/mol), thus making it more favorable for oxide formation. This high oxygen vacancy concentration at the Hf/oxide interface could facilitate low SET-

RESET voltage and resistance uniformity. By changing the pulse width, we were able to modulate resistance gradually, yet each resistance level was distinct and discrete without any overlap.

Beyond memory applications, RRAM also holds promise for use in performing logic functions,⁶ mimicking neuromorphic activities,⁷ physically unclonable function (PUF) based hardware encryption,⁸ or signal processing.⁹ One challenge for implementing RRAM for these applications is the significant programming variation in RRAM resistance states, which includes cycle-to-cycle variation and stochastic switching, producing unwanted bit flip. In this work, we have demonstrated excellent cycle-to-cycle uniformity for the absolute value of the high resistance states (HRS) and the low resistance states (LRS).

In this study, resistive switching memory (RRAM) devices were fabricated as follows. Pt bottom electrodes with 50 nm thickness were deposited on a Ti/SiO₂/Si substrate by direct current (DC) sputtering. A 3 nm TaO_x film was deposited using a radio frequency (RF) magnetron sputtering system (Kurt Lesker PVD sputtering system) in a process gas mixture of Ar and O₂ with a flow ratio of 3:1, followed by another 8 nm layer of TaO_y with an Ar and O₂ flow ratio of 4:1. The base pressure and the working pressure for the deposition were 1 × 10^{−7} Torr and 3 × 10^{−3} Torr, respectively. The deposition of tantalum oxide was carried out at 125 W RF power. Hence, the tantalum oxide layer adjacent to the bottom electrode (TaO_x) was more stoichiometric than the tantalum oxide layer (TaO_y) on the top of it. As a result, the top oxide layer maintained a higher oxygen vacancy concentration and acted as an oxygen vacancy reservoir, and the lower oxide layer was mainly involved in switching. Finally, a 3 nm oxygen gettering layer of Hf and 50 nm thick top electrodes of W were deposited by DC sputtering. These top electrodes were subsequently defined by contact photolithography and a lift-off process. The size of the top electrodes varied from 25 × 25 μm² to 100 × 100 μm². An Agilent B1500 semiconductor device analyzer was used to measure

FIG. 1. (a) Schematic of the device showing the material stack and relative thickness of each layer. (b) I-V switching characteristics of the device.

FIG. 2. (a) Thirteen different resistance levels were reached by changing the RESET pulse width, while keeping the SET/RESET voltage height and SET pulse width fixed. Each resistance level was maintained for 10^5 consecutive switching pulses. Level one corresponds to ON state resistance. (b) Different resistance levels were also achieved by changing the RESET voltage height and keeping other parameters fixed.

the current-voltage characteristics in the voltage sweep mode. A transistor was integrated by connecting the drain with the bottom electrode (BE) and the source with ground. The top electrode (TE) was biased by applying SET and RESET voltages. The read voltage used for repeat measurements was 0.2 V. The schematic drawing of the device and measurement setup is shown in Fig. 1(a).

Figure 1(b) shows a typical DC I-V curve of a $25 \times 25 \mu\text{m}^2$ W/Hf/TaO_y/TaO_x/Pt structure. A soft breakdown (forming step) was achieved usually by applying a voltage higher than SET voltage (5.5 V to 6 V) before the start of device switching. To achieve multilevel pulse-based switching, initially we applied fixed SET voltage with a fixed pulse width (2.6 V/10 μs) to a $25 \times 25 \mu\text{m}^2$ device and gradually varied the RESET pulse width from 10 μs up to 80 μs, keeping the pulse amplitude fixed at -3.3 V. A non-destructive read pulse of 0.2 V was applied after each SET and RESET pulse to measure the resistance of the device. The ON-state

resistance level was about 2 kΩ. The device was cycled at each resistance level 10^5 times. Thirteen discrete resistance levels were demonstrated, as shown in Fig. 2(a). A saturation effect in the OFF state (HRS) was observed as the pulse width was increased, starting at approximately 40–50 μs. We then increased the pulse height to -3.33 V, -3.35 V, and -3.38 V while keeping the pulse width at 80 μs. A drastic increase in resistance occurred in an exponential fashion as we increased the pulse height [Fig. 2(b)]. The $R_{\text{off}}/R_{\text{on}}$ ratio increased up to 10^3 as the RESET pulse height was modulated. Figures 3(a) and 3(b) show the relationship between pulse width and R_{off} and between voltage level and R_{off} . From these data, it can be inferred that the R_{off} can be tuned gradually, by incremental changes to the RESET pulse width. Further, devices exhibited excellent uniformity of resistance at each resistance level (10^5 cycles per level). With such discrete behavior, resistance states can be modulated precisely, making it possible to achieve quasi-analog behavior of the device, which is important for

FIG. 3. (a) Average RRAM device resistance state (from Fig. 2) was plotted against varying RESET pulse width (a) and RESET pulse height (b).

FIG. 4. (a) Cumulative distribution of resistance levels for pulse width modulation and (b) Cumulative distribution of resistance levels for pulse height modulation.

neuromorphic applications.¹⁰ No read errors were observed during repeat switching within each level, and no overlap was found between different resistance states. There was almost no cycle-to-cycle variation in the ON state resistance for each level. The cumulative distribution of resistance of different levels achieved by modulating the pulse width and pulse height is shown in Figs. 4(a) and 4(b), respectively. These data demonstrate that for pulse width modulation, resistance at each level is very uniform. For pulse height base resistance levels, only the 3.38 V RESET voltage yielded high resistance state variability.

Excellent endurance was obtained with the devices fabricated in this study, with up to 10^8 switching cycles achieved with pulse-based switching. As can be seen in Fig. 5(a), devices could be switched ON by applying a positive pulse of +2.6 V/20 μ s and switched OFF by a negative pulse of 2.8 V/50 μ s for the endurance test. The R_{off}/R_{on} ratio was 20:1 throughout these cycles, demonstrating stable performance. The retention properties of the devices are shown in Fig. 5(b). Devices were set to HRS and LRS, and resistance vs. time was measured with a 0.1 V pulse every 100 s, for each resistance state. The resistance level was maintained for longer than 10^4 s at room temperature, without any noticeable degradation, which indicates good retention properties.

To understand the conduction mechanism of these devices, I-V data were plotted (up to the SET point) as $\ln(J/T^2)$

versus $\sqrt{E}$, following the Schottky emission equation [Fig. 6(a)] and $\ln(J)$ versus $1/E$, following the trap assisted tunneling (TAT) equation [Fig. 6(b)]. Other conduction mechanism equations such as F-N tunneling and P-F tunneling were plotted but did not fit well with measured I-V data. HRS current conduction in the lower voltage region (up to 0.73 V) was found to be dominated by Schottky emission. In the higher voltage regime (>0.8 V), a straight line fit with a negative slope in the TAT plot indicated that a transition in current conduction from Schottky emission to trap assisted tunneling took place. The extracted barrier height (using the Schottky emission equation) was 0.58 eV, while the trap height extracted using the TAT equation was about 0.2 eV. We postulate that as positive bias is applied at the top electrode (negative bias at the bottom electrode), positively charged oxygen vacancies are attracted to the bottom electrode/oxide interface, modulating the Schottky barrier. As oxygen vacancies are effectively donors, the increase in the oxygen vacancy concentration at the metal-oxide interface will reduce the Schottky barrier width. This is due to the fact that the width of the Schottky barrier is inversely proportional to the square root of the dopant concentration.¹¹ As a result, a transition in current conduction takes place. Additional biasing further causes reduction in the barrier width, and direct tunneling becomes favorable; thus, the device switches from HRS to LRS through a transition from Schottky emission to

FIG. 5. Switching endurance of RRAM devices demonstrated for 10^8 cycles is shown in (a), while memory retention at an intermediate resistance level up to 10^4 s is shown in (b).

FIG. 6. (a) I-V plot for RRAM conduction was fit to the Schottky emission equation, with goodness of fit up to 0.73 V (marked by red dotted line). (b) Trap assisted tunneling (TAT) plot of I-V data with goodness of fit shown in the higher voltage ($V > 0.8$ V) region, shown in the inset.

tunneling. To further clarify the switching mechanism, we measured the temperature dependence of device current in both the LRS and HRS. In the HRS, conductance increased with the temperature and a $\ln(I/T^2)$ vs $1/T$ plot exhibited a linear relationship with the negative slope [Fig. 7(a)], which further suggests Schottky emission during HRS. In LRS, however, there was almost no discernible change in conductance as temperature was increased [Fig. 7(b)], suggesting tunneling based conduction, since this mechanism is generally temperature independent or very weakly temperature dependent.¹¹

We have demonstrated resistance modulation by changing the RESET pulse width with tantalum oxide based RRAM devices. We performed SET-RESET switching for each resistance level 10^5 times, showing excellent endurance behavior for each level. Several research groups have demonstrated MLC operation in TaO_x based RRAM, mostly by changing the peak current compliance during switching¹² or by changing the RESET stop voltage and RESET pulse height.⁴ Hu *et al.* have shown multi-level resistance with TaO_x based RRAM through controlling different RESET stop voltages and different compliance currents in direct current voltage sweeping modes and by means of different pulse erasing voltages in pulse programming/erasing modes.¹³ In many cases, individual resistance levels were not switched for a sufficient number of cycles, and many of the resistance states exhibited large variation. In this study, when using bilayer TaO_x based RRAM with Hf as the OEL, each resistance level was uniform and non-overlapping and hence is suitable for applications where cycle to cycle uniformity is of utmost importance. We propose two possible reasons for

this uniformity. First, the μs timescale for pulse applications could be helpful for achieving stable and uniform resistance levels. In particular, we observed that shorter RESET pulse widths were associated with reduced resistance variability [Figs. 2(a) and 4(a)]. Second, the Hf OEL and substoichiometric TaO_x layer may have led to a higher concentration of oxygen vacancies, which in turn could induce higher vacancy movement and facilitate more uniform resistance levels. For oxygen vacancy concentrations greater than a certain level, the local lattice becomes distorted and strained, leading to a greatly increased diffusion constant for oxygen vacancies.¹⁴ These devices also show good endurance and retention and high $R_{\text{off}}/R_{\text{on}}$ ratio for longer cycles. For a fixed RESET pulse height, a change in the pulse width caused a gradual change in the resistance level. Changing the pulse height while keeping the pulse width fixed, however, caused a drastic change in R_{off} . These results demonstrate multilevel storage capability and suggest that our devices are amenable to applications such as neuromorphic computing and hardware based encryption systems. Finally, based on the electrical measurement results, curve fitting, and temperature based study, we suggest that Schottky emission dominates at the HRS, while trap assisted tunneling dominates at higher voltages, and the device switches from HRS to LRS through a transition from Schottky emission to tunneling.

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FIG. 7. (a) RRAM device current in the high resistance state (OFF) increased with temperature, following a Schottky emission mechanism. (b) Device current was independent of temperature dependence for the low resistance state (ON).

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