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Substrate dielectric effects on graphene field effect transistors

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Graphene is emerging as a promising material for future electronics and optoelectronics applications due to its unique electronic structure. Understanding the graphene-dielectric interaction is of vital importance for the development of graphene field effect transistors (FETs) and other novel graphene devices. Here, we extend the exploration of substrate dielectrics from conventionally used thermally grown SiO₂ and hexagonal boron nitride films to technologically relevant deposited dielectrics used in semiconductor industry. A systematic analysis of morphology and optical and electrical properties was performed to study the effects of different substrates (SiO₂, HfO₂, Al₂O₃, tetraethyl orthosilicate (TEOS)-oxide, and Si₃N₄) on the carrier transport of chemical vapor deposition-derived graphene FET devices. As baseline, we use graphene FETs fabricated on thermal SiO₂ with a relatively high carrier mobility of 10 000 cm²/(V s). Among the deposited dielectrics studied, silicon nitride showed the highest mobility, comparable to the properties of graphene fabricated on thermal SiO₂. We conclude that this result comes from lower long range scattering and short range scattering rates in the nitride compared those in the other deposited films. The carrier fluctuation caused by substrates, however, seems to be the main contributing factor for mobility degradation, as a universal mobility-disorder density product is observed for all the dielectrics examined. The extrinsic doping trend is further confirmed by Raman spectra. We also provide, for the first time, correlation between the intensity ratio of G peak and 2D peak in the Raman spectra to the carrier mobility of graphene for different substrates. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4879236>]

I. INTRODUCTION

Graphene, the exemplary 2-D material with excellent electronic,^{1–3} optical,^{4,5} and thermal transport⁶ properties holds promise for radio frequency applications and novel nanoelectronic concepts such as “electron optics” devices.^{7,8} Mobility of carriers greater than 10⁶ cm²/(V s)⁹ has been achieved by suspending exfoliated graphene flakes and driving off the impurities. However, chemical vapor deposition (CVD)-derived graphene supported on technologically relevant dielectric substrates has relatively low room temperature (RT) mobility of ~10³ cm²/(V s).¹⁰ Given the very weak electron-phonon coupling in graphene of up to 400 K,¹¹ the degradation of the electrical transport properties has been attributed to disorder in the graphene and environmental effects, including charged impurities,^{12,13} remote optical phonons,^{14,15} lattice defects,¹⁶ surface roughness,¹⁷ and resonant scattering centers.¹⁸

Recently, hexagonal boron nitride (h-BN) was identified as a substrate that allows high graphene mobility (as high as ~40 000 cm²/(V s))^{19,20} because it is atomically flat and is free of dangling bonds and charge traps. Unfortunately, single-crystalline h-BN is not currently available in large area.

To allow the integration of graphene for both active and passive circuit components, deposited dielectric films that allow high mobility are needed. It was reported that depositing high- κ dielectric on graphene could enhance the mobility by reducing remote charge impurity scattering,²¹ while other

groups predicted surface phonon modes arising from the high- κ dielectric would wash out this advantage.^{14,22} Therefore, we have set-out to develop a better understanding of scattering mechanisms on technologically relevant deposited dielectric substrates, including high- κ films.

Our benchmark structure is graphene on thermally grown SiO₂, where we have achieved high RT mobility (10 000 cm²/(V s)) by optimizing the graphene growth and transfer processes. Using graphene on thermally grown SiO₂ as base line, we systematically examine the properties of graphene devices fabricated on several technologically relevant substrates (HfO₂, Al₂O₃, tetraethyl orthosilicate (TEOS)-oxide, SiO₂, Si₃N₄). We examined over 8 devices per substrate. We present representative data and, where possible, we also show their ranges.

II. EXPERIMENTAL

Graphene was synthesized on copper foils using a CVD growth technique in a commercially available hot walled quartz tube (2.5 in. diameter) furnace (Firstnano Easytube 3000). The starting material was a 25 μ m thick copper foil (99.8%, Alfa Aesar). It was cleaned in acetone and isopropanol (IPA) sonic bath for 3 min each, followed by soaking in acetic acid for 30 min to remove surface oxide. It was rinsed in deionized (DI) water and dried by N₂ prior to loading it into the quartz furnace. Next, we evacuated the furnace to 1 mTorr and filled with H₂ (50 sccm) and Ar (80 sccm) and pre-annealed at 1035 °C for 1 h to further clean the surface and increase the Cu grain size. For growth, a mixture of Ar (120 sccm), H₂ (7 sccm), and methane (5 sccm) was

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introduced into the tube at 1035 °C for 3 min at 200 m Torr. Keeping the same temperature and the pressure, the mixture was altered to H₂ (10 sccm) and methane (50 sccm) for 50 min for further growth. Finally, the furnace was cooled down slowly to 60 °C in H₂ and Ar.

Graphene on the backside of the Cu foil was etched away by oxygen plasma before its transfer on to substrates. The transfer process started with spin coating of poly(methyl methacrylate) (PMMA) (950 A4) at 2500 rpm on the graphene, followed by the application of a thermal release tape with a predefined window cut into the tape. The copper substrate was etched in ammonia persulfate. The suspended graphene/PMMA within the tape window was cleaned with DI water and dried in IPA vapor. The completed stack was then applied onto the substrate. On a smooth surface, such as thermally grown SiO₂, graphene can be brought into intimate contact with SiO₂ after heating to 130 °C to release the tape. For rough surfaces, such as in deposited CVD oxide (TEOS), the substrate was ramp heated on a hot plate slowly from 100 °C to 160 °C and kept at 160 °C for 5 min. All samples were cooled in air and eventually the PMMA was removed using acetone.

Graphene field effect transistors (FETs) devices were fabricated using a conventional photolithography process. First, graphene was patterned using a positive photoresist, followed by etching of unwanted graphene regions by oxygen plasma. Second, the electrodes were patterned on graphene using image reversal photoresist, followed by metal evaporation and lift-off process.

All electrical data were measured using Keithley S4200 in a Lakeshore vacuum-cryostat probe station at room temperature, after an in-situ annealing at 122 °C for 4 h in vacuum atmosphere of 10⁻⁵ Torr. The Raman spectra were

acquired after electrical measurements using HORIBA JOBIN YVON LabRAM HR 800 Raman spectrometer with a 532 nm laser excitation source. Atomic force microscope (AFM) images were obtained from scanning probe station with a tapping mode tip (Nanosensors PPP-NCH-10).

III. RESULTS AND DISCUSSION

Large-area polycrystalline graphene was grown on copper foils using a CVD technique following a two-step²³ and extended time²⁴ growth procedure. A number of different techniques have been reported in the literatures to transfer the graphene onto a substrate. A water-based transfer procedure is frequently used. This transfer process, however, has been reported to cause degradation in electrical properties, which could be mitigated by using IPA¹⁰ instead of water. A possible cause for this degradation is trapped water molecules or inadvertent incorporation of chemical residuals between graphene and the substrate during the aqueous transfer process. Another procedure uses thermal release tape. We found, however, that a dry transfer process²⁵ using thermal release tape left tape residuals on graphene.

In the present work, we avoided these problems by using the following procedure that yielded devices with high mobility: After spinning on a layer of PMMA onto graphene and etching the copper substrate, we dried the graphene prior to transferring it onto different substrates. A similar dry transfer method²⁶ has been demonstrated to provide graphene with high carrier mobility. All the substrates used in this work were deposited in our 300 mm semiconductor wafer line. They are: 5 nm Atomic Layer Deposited (ALD) HfO₂ on 100 nm thermal SiO₂; 5 nm ALD Al₂O₃ on 100 nm thermal SiO₂; 100 nm Plasma Enhanced Chemical Vapor

FIG. 1. Roughness of substrates and graphene on substrates. (a) AFM images of different substrates. (b) AFM images of graphene transferred onto different substrates (scale bar, 1 μ m; color bar, ± 3 nm). (c) Gaussian fit of the height distribution for the different substrates with and without the graphene.

Deposition (PECVD) TEOS-SiO₂; 100 nm thermal SiO₂; and 90 nm PECVD Si₃N₄. The dielectric constant of the substrate materials varies from ~ 3.9 to ~ 22 .

To analyze the properties of graphene on these substrates, we first investigated the morphology and its impact on the adhesion properties of graphene by taking AFM images in the tapping mode. Figs. 1(a) and 1(b) show the surface topography images with and without the graphene, respectively. The height distribution of these topography images can be fitted well by a Gaussian function and they are shown in Fig. 1(c). The roughness of the surface was characterized by the standard deviation σ of the height distribution, which is given by full-width at half-maximum (FWHM) divided by 2.36. For all the as-deposited substrates, the surface roughness is estimated to be approximately 0.3–0.45 nm, except TEOS which had a value of 1 nm. The roughness increases slightly after transferring graphene onto the substrates, which might be caused by chemical residuals. Because of the relatively narrow variation in σ among the substrates (except TEOS), we exclude strain arising from surface roughness as a possible cause of the variations we report below. As seen in Fig. 1, graphene on thermal SiO₂ and Si₃N₄ showed relatively smooth surface morphology, while graphene on HfO₂ and Al₂O₃ showed regions with wrinkles. The wrinkles typically have a height of about 4 nm and a separation of a few hundred nanometers. Although some have proposed that wrinkles²⁷ are an intrinsic morphology of graphene when it is grown on Cu foil, our study suggests that other factors, such as the type of substrates and transfer methods, also contribute to their formation. These wrinkles can lead to anisotropic transport along and across the wrinkles,²⁸ and thus HfO₂ and Al₂O₃ may not be preferred from this stand point. Our study also suggests that surface roughness has a large impact on graphene adhesion. We observe lots of tears in graphene, which lowers device yield, when it is placed on the TEOS substrate. Thus, we suggest that substrates with surface roughness greater than 1 nm are

not suitable for high performance graphene device applications. Although we include the data from TEOS, we do not analyze them in detail due to low device count.

We now examine the electrical transport properties of graphene FETs fabricated on the different substrates. The conditions used to test these devices are described in the experimental section. In order to eliminate run-to-run variations, the graphene films used in these measurements were taken from the same batch. All graphene FETs, shown in Fig. 2(a), are patterned into 8 μm long and 4 μm wide channels. Fig. 2(a) shows the conductivity σ plotted against the carrier density n induced by the back gate, offset by the charge neutrality point ($n_g - n_{\text{CNP}}$). The bias was adjusted to achieve a similar range in the induced carrier density for the different substrates. To accurately measure the carrier density, we also measured the capacitance. We obtained 35.71, 34.14, 36.06, 34.52, and 68.83 nF/cm² for HfO₂, Al₂O₃, TEOS, SiO₂, and Si₃N₄ films, respectively, which are close to their theoretical values. As Fig. 2(a) shows different substrates have significantly different electrical behavior.

We fit the sub-linear behavior of $\sigma(n)$ using a model that incorporates randomly distributed Coulomb impurity and short range scattering mechanisms,^{29,30} as described by Eq. (1). This model captures the important aspects of graphene transport, including the minimum conductivity around the charge neutrality point, linear density-dependent conductivity above the puddle-density dominated regime, and sub-linear density-dependent conductivity at higher carrier density. By fitting our data to Eq. (1), we extract three parameters, which are discussed below

$$\sigma^{-1} = \left(q\mu_L \sqrt{n^2 + n_0^2} \right)^{-1} + \rho_{sc}. \quad (1)$$

Here, n_0 is the intrinsic carrier density, μ_L is the density-independent mobility from long range scattering, and ρ_{sc} is the resistivity contribution from short range scattering

FIG. 2. Representative transport curves of graphene FETs on different substrates using a 4-point transport measurement. (a) Circles show carrier density dependent conductivity. Solid lines are fits to Eq. (1). Carrier density was calculated by using $n = C(V_g - V_{\text{CNP}})/q$. In (b)–(d), parameters extracted from the experimental data for different substrates are plotted against the dielectric constant κ , solid circles and open circles represent electron and hole data, respectively. (b) density-independent mobility, (c) intrinsic carrier density, and (d) the resistivity contribution from short range scattering processes. In (d), a trend line was added to show the linear relation between the short range scattering and the dielectric constant.

FIG. 3. Intrinsic carrier density vs. density-independent mobility, showing an overall constant product between μ_L and n_0 indicated by the dashed line. Solid dots represent electron data. Circles represent hole data. Inset: The ratio of μ_{Le} to μ_{Lh} versus different substrates. Error bars represent experimental error in calculating the mobility ratio from the fitting procedure.

processes. This model fits the experimental data for all the substrates we have examined. They are shown as solid lines in Fig. 2(a). Since we used identically processed graphene, we associate the variation in the transport properties to the variation in the parameters in Eq. (1), which are particular to each substrate.

In Fig. 2(b), μ_L is significantly higher for graphene on SiO_2 and Si_3N_4 than on HfO_2 and Al_2O_3 . Concomitantly, the intrinsic carrier density is lower for graphene on SiO_2 and Si_3N_4 than on HfO_2 and Al_2O_3 , as we show in Fig. 2(c). Using these values, we plot density-independent mobility, for both holes and electrons, against the intrinsic carrier densities for different substrates in Fig. 3(a). We find that the product of density-independent mobility and intrinsic carrier density is a constant for the substrates we examined, with $\mu_L \times n_0 \approx 2.56 \times 10^{15} / (\text{Vs})$, which is the central result of our work. This implies a universal behavior between density-independent mobility, primarily arising from long range scattering mechanisms, and density fluctuations near the charge neutrality point. The long-range disorder could come from charged impurities.^{12,31,32} The difference in the substrate-dependent charged impurities could be explained by the variation in the surface chemistry³³ or electronic defects introduced during film deposition processes.³⁴

We also observed the presence of conduction asymmetry^{12,35} in all our graphene devices. This results in a difference between electron and hole mobility values, with an average electron-to-hole mobility ratio of ~ 0.8 for SiO_2 , Si_3N_4 , and Al_2O_3 and a lower value of ~ 0.54 for HfO_2 , as shown in the inset of Fig. 3(a). Most of our graphene devices show negative shift in Dirac point, indicating that there are more positively charged impurities than negatively charged impurities in the system. In one report, it is shown that positively charged impurities scatter electrons more effectively than holes.³⁶ Thus, the asymmetry in mobility can be attributed to the asymmetry in scattering rate that preferentially

scatters electrons more than holes,³⁷ although further studies are needed to study the origin of these scatterers. Here, we limit our discussion to the hole branch where we observe higher mobility but a notable difference in ρ_{sc} for different substrates. In Fig. 2(d), we show that ρ_{sc} for hole branch increases linearly with increasing κ . It is understood that the conductivity of graphene at high-density regime is nonuniversal³⁸ with substrates, where many scattering mechanisms compete depending on the disorder density range.³¹ In our data, the contribution of ρ_{sc} to the resistivity of graphene at high-density regime ranges from about 50%, for SiO_2 , to about 80%, for HfO_2 , suggesting that this is the dominant scattering mechanism over the long range scattering. Thus, we attribute the differences in ρ_{sc} to variations in the short range scattering, which is likely related to polar optical phonon scattering, from the substrates. The resistivity due to short range scattering has similar values for graphene on SiO_2 and h-BN, although the exact mechanism for the short range scattering is still not known.¹⁹ The similarity in their resistivity values should be compared to the similarity in the values of their static dielectric constants. In general, the higher the static dielectric constant, the higher is the phonon scattering rate.²² Thus, we attribute the increase in ρ_{sc} with increasing dielectric constant to the increased surface optical phonon scattering rates from the substrates. Furthermore, Al_2O_3 and HfO_2 have much lower activation energy for surface-phonon modes while Si_3N_4 has the same activation energy as that for h-BN. We conclude that high- κ dielectric films are not favored due to the high charged impurities and high short range scattering rates. We also conclude that Si_3N_4 is the best dielectric substrates for graphene among the technologically important dielectric substrates we have investigated.

Finally, a systematic study of Raman spectra on graphene channels on different substrates is shown in Fig. 4. The Raman spectra were taken on the same devices used for the electrical measurements. Fig. 4(a) shows representative Raman spectra after normalizing them to the 2D peak height. The characteristic peaks of graphene are the D peak near $1300\text{--}1350\text{ cm}^{-1}$, the G peak near $1580\text{--}1590\text{ cm}^{-1}$, and the 2D peak near $2600\text{--}2700\text{ cm}^{-1}$.³⁹ The G and 2D peaks provide information on doping, layer number, and strain, and the D peak is only activated in graphene with lattice defects.⁴⁰ The D peak is very small on all the substrates we examined, indicating that the graphene quality is high. In order to obtain a more quantitative understanding, statistical analysis of the peak parameters (Table I) was performed, which were based on 15–20 spectra from each substrate and fitting of these peaks to a Gaussian function.

Scatter plots of the Raman peak parameters are shown in Figs. 4(b) and 4(c). In Fig. 4(b), the G and 2D peak positions (ω_G and ω_{2D}) are plotted. The G peak is upshifted for all the substrates from the G peak position of an undoped graphene.³⁹ Only TEOS substrates show results indicative of an undoped graphene, although the scatter in the data is large. Generally, the upshift of the G peak position in the Raman spectra is ascribed to doping⁴¹ or compressive strain.⁴² However, a compressive strain for graphene supported on thermally grown SiO_2 was reported to be very

FIG. 4. Raman spectra of graphene on different substrates and peak parameter analysis. (a) Representative Raman spectra of graphene on different substrates, normalized to 2D peak height. Raman spectra were taken in air at 532 nm laser excitation wavelength. (b) and (c) Scatter plots of Raman peak parameters. (b) 2D peak position (ω_{2D}) vs. G peak position (ω_G). (c) I_{2D}/I_G intensity ratio vs. G peak position (ω_G).

small.⁴³ Thus strain can be ruled out as the cause of the difference in the peak positions for SiO₂, Si₃N₄, HfO₂, and Al₂O₃ substrates given the similarity in the surface roughness, as seen in Fig. 1(b). The simultaneous upshifts of G peak and 2D peak can therefore be solely explained by doping from the interfacial properties of the substrates. Specifically, the Raman data suggest smaller doping for SiO₂ and Si₃N₄, and larger doping for HfO₂ and Al₂O₃. However, on TEOS, the downward shift for both the G and 2D peak positions, likely caused by strain,⁴² can be attributed to the roughness of the substrate. We also attribute the larger variation in the peak parameters to the rough surface. The peak intensity ratio I_{2D}/I_G plotted against the G peak position in Fig. 4(c) confirms the increased doping trend we observe with different substrates, in the following order of increased doping: SiO₂, Si₃N₄, HfO₂, and Al₂O₃.

The increased doping also leads to stiffening of the G-band,⁴⁰ which is shown in the FWHM of its peak (Γ_G) in Table I. On the other hand, a higher value of FWHM of the 2D peak (Γ_{2D}) was proposed to correlate with higher amplitudes of charge fluctuations³³ due to electron-hole puddles. The size of such electron-hole puddles for graphene on SiO₂ has been measured to be ~ 20 nm in diameter⁴⁴ by scanning

tunneling spectroscopy. Thus, Si₃N₄ could have similar sizes of electron-hole puddles as SiO₂, and Al₂O₃ may have even smaller puddle sizes.

To shed further light, we explore the correlation between electrical properties and Raman spectra. Intensity ratio I_{2D}/I_G and the peak position of G peak are plotted against density-independent mobility in Fig. 5(c). The Raman peak intensity ratio I_{2D}/I_G and the G peak position strongly correlates to the graphene hole mobility. Graphene on SiO₂ has the highest I_{2D}/I_G ratio and the least upshift in ω_G . This is indicative of low doping and leads to the highest observed mobility. Next, substrates in the order of decreasing mobility are Si₃N₄, HfO₂, and Al₂O₃. Both higher I_{2D}/I_G and less upshift indicate less doping level in the graphene film. Therefore, we conclude that carrier mobility of graphene is dominated by doping. This conclusion agrees well with our earlier argument in Fig. 3 that mobility is limited by intrinsic carrier density in graphene.

TABLE I. Summary of average graphene Raman peak parameters and mobilities.

Substrate	ω_G^a	Γ_G^a	ω_{2D}^a	Γ_{2D}^a	I_{2D}/I_G	μ_{Lh}^b
SiO ₂	1586.1	11.9	2677.6	33.2	2.22	9147
Si ₃ N ₄	1588.2	10.5	2677.5	33.2	2.10	8600
HfO ₂	1590.1	9.1	2679.2	31.6	1.89	5980
Al ₂ O ₃	1594.2	9.6	2682.4	34.6	1.32	4940
TEOS	1585.1	16.6	2674.5	36.1	2.85	3685

^aUnit is cm⁻¹.

^bUnit is cm²/(V s).

FIG. 5. Carrier density independent hole mobility vs. intensity ratio I_{2D}/I_G (solid dots) and the peak position of G peak ω_G (circles). Two guide lines are added to show the trends.

IV. CONCLUSIONS

In summary, we have studied the effects of technologically relevant substrates on the transport properties of CVD derived graphene-based FET devices, produced using an optimized dry transfer and fabrication processes. The substrates influence the morphology of graphene, the doping, and the scattering of carriers. Thermally grown SiO₂ substrate produced the highest mobility. Among the deposited films, Si₃N₄ proved to be the most suitable substrate for graphene, compared to Al₂O₃, HfO₂, and TEOS-oxide, which were the other substrates we examined. We found clear correlation on hole mobility to impurity density and short range scattering. A universal product of mobility and intrinsic carrier density was observed for all the substrates, which implies that the carrier mobility in graphene is largely limited by charged impurities. This dependence was also confirmed in the Raman spectra. On different substrates, we found the mobility to increase with increasing intensity ratio of I_{2D}/I_G and a redshift of G peak position. This relation can be used as a simple measure to determine the quality of substrates and surface treatment on the electrical properties.

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