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Interface trap density and mobility extraction in InGaAs buried quantum well metal-oxide-semiconductor field-effect-transistors by gated Hall method

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In this work, we are using a gated Hall method for measurement of free carrier density and electron mobility in buried InGaAs quantum well metal-oxide-semiconductor field-effect-transistor channels. At room temperature, mobility over 8000 cm²/Vs is observed at $\sim 1.4 \times 10^{12}$ cm⁻². Temperature dependence of the electron mobility gives the evidence that remote Coulomb scattering dominates at electron density $< 2 \times 10^{11}$ cm⁻². Spectrum of the interface/border traps is quantified from comparison of Hall data with capacitance-voltage measurements or electrostatic modeling. Above the threshold voltage, gate control is strongly limited by fast traps that cannot be distinguished from free channel carriers just by capacitance-based methods and can be the reason for significant overestimation of channel density and underestimation of carrier mobility from transistor measurements. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4870257>]

Group III–V semiconductors are potential candidates for alternate channel materials replacing strained Si in digital integrated circuits. The benefits of III–V materials arise from their high carrier mobility due to low effective mass as compared to Si. Several research groups^{1–4} have reported that mobility is degraded at the III–V/high- κ interface due to a high density of interface traps (D_{it}). The D_{it} values^{5–9} at the In_{0.53}Ga_{0.47}As/high- κ interface evaluated using capacitance methods varies by ~ 2 orders of magnitude in different groups not only due to different technologies used but also due to variations in D_{it} extraction methodology. The spread of values is the widest at the conduction band edge because of low density of states and typically higher effect of border trap densities.

Typically border traps¹⁰ manifest a capacitance dispersion with frequency in accumulation. The trap response in accumulation or above the threshold voltage in quantum well (QW) channels can be very fast, and these fast traps are significantly less studied. The conventional trap extraction methods, based on capacitance or conductance response (capacitance-voltage (CV) methods) of MOS capacitors at frequencies < 1 MHz, cannot distinguish between conducting and trapped carriers. In addition, frequency dispersion in the accumulation region makes it a difficult task to measure the true oxide capacitance (C_{ox}) value. Another implication of these properties of III–V interfaces is an ambiguity in determination of electron density in the metal-oxide-semiconductor field-effect-transistor (MOSFET) channel. Traditional evaluation of carrier density by integration of the CV curve gives significantly overestimated results even if corrected for D_{it} . It happens because the CV methods distinguish free and trap carriers exclusively by their response kinetics, and therefore all trapped electrons responding faster than ~ 1 μ s are treated as free electrons.

In this work, we are using a gated Hall method for direct measurement of free carrier density in a buried InGaAs quantum well MOSFET channel, and electron mobility. When combined with CV measurements or electrostatic

modeling, it allows for accurate quantification of D_{it} spectrum above and below the conduction band minimum.

The MOS gated Hall structures with 10 nm In_{0.77}Ga_{0.23}As compressively strained buried QW channels were grown by molecular beam epitaxy on semi-insulating InP(100) substrates as shown in Fig. 1 with a corresponding band structure in Fig. 2. The channel was grown on 85 nm thick In_{0.53}Ga_{0.47}As barrier and buried with 3 nm-In_{0.52}Al_{0.48}As/2 nm-In_{0.53}Ga_{0.47}As barrier (5 nm total). Modulation doping using Si δ -doping layer was placed 3 nm above the QW. Gate oxide, 10 nm Al₂O₃, was grown *in-situ* at room temperature by thermal evaporation of Al in pure O₂ at a pressure of about 1.5×10^{-6} Torr. The gate oxide was further annealed at 450 °C for 10 min in forming gas followed by gate metal (TiW) sputter deposition.

The fabrication of a gated Hall device involved 5 lithographical steps starting with gate patterning. Ohmic contacts to the QW were formed by lift-off of an e-beam evaporated Pd/Ge metal stack onto HCl:H₂O (1:1) cleaned semiconductor and subsequently annealed at 400 °C in forming gas. In order to reduce leakages in the structure, the gate pad and active gate area were separated by a reactive ion etched trench which was further filled with Durimide-32A. This polymer provides isolation with low shrinkage upon cure and good mechanical properties. Final Au gate metallization was evaporated and lifted-off over the planarized polymer, gate pad, and active gate area.

Two kinds of gated Hall structures were fabricated, with Van der Paw (VdP) (Fig. 1, inset) and with double Hall-cross bar configuration. Although the results are similar in these two types of structures, the difference arises from higher potential drop over the Hall bar. The VdP configuration provides more uniform carrier density under the gate and more accurate determination of the carrier density and sheet resistivity vs. gate potential at low (subthreshold) channel currents. Therefore, the VdP results will be presented.

Impedance gain-phase analyzer is used for split capacitance-voltage characteristics measurements. Hall and

FIG. 1. Cross-section of a gated Hall structure with buried $\text{In}_{0.77}\text{Ga}_{0.23}\text{As}$ QW. Inset: Top view of a trench-isolated $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ Van der Pauw device.

resistivity data were obtained at temperatures down to 77 K in a magnetic field up to 1 T on wire-bonded structures. Hall factor was assumed to be equal to one.

Fig. 2 shows Schrodinger-Poisson (SP) simulation of the band structure illustrating the bending of the conduction band edge for three gate biases assuming no interface traps (IT) present in the structure. The expected position of the IT is also shown in Fig. 2. Free carrier density and sheet resistivity in the QW as a function of gate bias obtained from Hall and resistance measurements in the temperature range 135–300 K are plotted in Fig. 3. The electron density curves provide data to calculate a “true” subthreshold swing, SS, which is not affected by possible mobility changes as in MOSFET drain current measurements. The SS allows for rough estimation of the interface trap density (D_{it}) close to the conduction band edge. The subthreshold swing reduces at low temperature as shown in the inset of Fig. 3(a), and the slope corresponds to $D_{it} \sim 1.3 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$.

The dependence of Hall mobility (μ) on sheet density (Fig. 4) is extracted simultaneously from the presented data. At room temperature, mobility over $8000 \text{ cm}^2/\text{Vs}$ is observed at $\sim 1.4 \times 10^{12} \text{ cm}^{-2}$. Similar to the recently observed behavior in gate-less structures,^{1,11} the mobility curve shows a maximum at density $(1\text{--}2) \times 10^{12} \text{ cm}^{-2}$. The extracted high mobility values above the transistor threshold reveal

FIG. 2. Simulated bands structure showing conduction band edge (E_C) bending for three gate biases: E_F —Fermi level, IT—interface traps.

FIG. 3. (a) Sheet density and (b) sheet resistance as a function of gate bias for the temperature range 135 K–300 K obtained using Hall measurements. The inset shows the evolution of SS with temperature. Solid lines are drawn for two interface traps densities, $qD_{it} = (SS/60 \text{ meV} - 1)C_{ox}$, with $C_{ox} = 0.8 \text{ }\mu\text{F}/\text{cm}^2$.

that there is a relatively weak interface/oxide related scattering in this buried channel structure. The mobility values of $11\,000\text{--}13\,000 \text{ cm}^2/\text{Vs}$ in similar QWs far from the interface were reported at room temperature.²

FIG. 4. Hall mobility as a function of sheet electron density for the temperature range 135 K–300 K. Note the change of density scale from log to linear. Inset illustrates the change of slope of $\mu(T) \sim T^\alpha$, from $\alpha = -1$ to $+1$ with electron density.

On the other hand, at low electron densities the mobility decreases significantly. At a density of $2 \times 10^{11} \text{ cm}^{-2}$, the temperature dependence of mobility reverses the slope (Fig. 4, inset), and therefore is clearly dominated by remote Coulomb scattering (RCS) from the interface.^{12,13} At higher densities, the electrons likely start occupying the high-effective mass L minimum. This temperature behavior is again very similar to that observed in the channels with gate oxide but without gate metal.¹¹

The carrier density determined by Hall measurements corresponds solely to free carriers in the QW, n_{QW} . An important fact observed in the Fig. 5 is that above the threshold voltage, free carrier density increases unexpectedly slow with a slope $0.33 \mu\text{F}/\text{cm}^2$, which is less than half of oxide capacitance and further decreasing at higher gate voltages. This behavior is illustrated in Fig. 5 by the plot of the channel capacitance, C_{QW} , and by the comparison of experimental and SP-simulated electron density in Fig. 5, inset.

As a result, the channel electron density is significantly less than that obtained by integration of the CV curves^{6–8} even at the highest frequency. This essential difference is due to re-charging of interface traps that are responding significantly faster than the measuring CV frequency of 1 MHz. The spectrum of these traps can also be determined as shown in Fig. 6. It is worth noting that these fast traps cannot be distinguished from free carriers by capacitance-based techniques, and might be the reason for significant underestimation of channel mobility^{6,14} values when the channel carrier density is determined by integration of CV curves.

Interface trap density, D_{it} , can be estimated using the obtained values of the channel electron density in two ways. The first method compares the electrostatic SP simulation of the channel carrier density with the density obtained from gated Hall measurements (inset of Fig. 5) as originally proposed by Fang and Fowler¹⁵ (SP/Hall method)

$$D_{it} = q \frac{\Delta Q_{it}}{\Delta \phi_s}, \quad \Delta Q_{it} = C_{ox}(\Delta V_{G,\text{exp}} - \Delta V_{G,\text{sim}}),$$

FIG. 5. Experimental capacitance-voltage characteristics measured at different frequencies and channel capacitance, $C_{QW} = dn_{QW}/dV_g$ extracted from room temperature electron density in Fig. 3(a). The inset shows the experimental and Schrodinger-Poisson simulation of electron density in the QW channel.

FIG. 6. Interface trap density values (D_{it}) extracted from Hall measurements using SP simulations (SP—large symbols) and using CV data at two frequencies (small symbols with lines) for two MOSFET samples: #1 with *in-situ* Al_2O_3 oxide and #2 with *ex-situ* ALD Al_2O_3 oxide. E_c corresponds to Fermi level crossing of the conduction band-edge of the top InGaAs barrier layer ($V_g = +0.2 \text{ V}$ in Fig. 2).

where $\Delta \phi_s$ is the change of the surface potential corresponding to the change in the interface charge density ΔQ_{it} , which is calculated from comparison of experimental, $\Delta V_{G,\text{exp}}$, and theoretical, $\Delta V_{G,\text{sim}}$, gate voltages that give the same channel carrier densities. C_{ox} is the oxide capacitance and q is the elementary charge. This method relies on an ideal simulated $n_{QW}(V_g)$ dependency, requiring detailed knowledge about the structure and the equivalent thickness of the gate oxide. The simulation also allows to link gate voltage to the surface potential provided the traps are located at the interface and/or in the oxide.

The second method^{9,11} utilizes the comparison of the channel capacitance, C_{QW} , to the measured MOS capacitance as shown in Fig. 5 (CV/Hall method). It is important that this method does not require the knowledge of oxide capacitance. The D_{it} spectra obtained by these two methods are shown for two samples in Fig. 6. The sample #1 as described above (Figs. 1–5) is compared to a similar structure but with an *ex-situ* atomic-layer deposited (ALD) Al_2O_3 gate oxide (#2). The latter sample has $\sim 2\text{--}3\times$ higher D_{it} values.

The CV/Hall method also allows for evaluating the trap response at each frequency. In this case, the D_{it} spectrum, extracted from Hall data and a CV curve obtained at a specific frequency, gives the density of all traps that respond faster than that frequency. As expected, SP/Hall trap spectra are in good agreement with the low-frequency CV/Hall results, and the values roughly correlate with the subthreshold swing derived from Fig. 3(a).

The trap spectra extracted from high-frequency CV/Hall data show very high values $(3\text{--}5) \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ close to E_c which correspond to trap response times less than $0.2\text{--}0.3 \mu\text{s}$. These traps cannot be distinguished from free channel electrons using just capacitance methods that typically utilize measuring frequencies limited at $1\text{--}2 \text{ MHz}$ by circuit parasitics.

The measured density of traps, D_{it} , also includes density of bulk oxide traps/border traps, projected to the interface. When the surface potential approaches and passes the band

edge, the trap response time reduces exponentially, and becomes very short down to ns. In fact, extremely fast border/interface traps have been observed recently using GHz-range transconductance method.¹⁶ These traps are believed to be located within ~ 3 Å from the oxide/semiconductor interface as estimated from tunneling border trap model.¹⁷ It should be noticed that even if additional semiconducting top barrier is placed between the channel and the oxide interface, the trap response is still faster than 1 MHz.

Electron density and mobility were measured in buried InGaAs MOSFET channel as a function of temperature with gated Hall method. The inversion of the slope $\mu(T) \sim T^\alpha$, gives the evidence for remote Coulomb scattering domination at electron density $< 2 \times 10^{11} \text{ cm}^{-2}$. Using extracted carrier density in the channel, the interface trap density (including border traps) is evaluated by two methods: from comparison to the simulated carrier density and to the CV data. A significant density of very fast (> 1 MHz) traps above the threshold gate voltage were measured. These trap states cannot be distinguished from free channel carriers just by capacitance-based methods and can be the reason for significant overestimation of channel density and underestimation of carrier mobility from transistor measurements.

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